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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,815	09/28/2000	Gregory A. Overkamp	10559/274001/P9281-ADI	9785

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FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 12/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/675,815	Applicant(s) OVERKAMP ET AL.	
	Examiner Henry W.H. Tsai	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/28/00* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ___ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, in claim 14, line 4-5, the "pre-decoder which determines the size and number of the plurality of instructions" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 16 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

In claim 16, "the predecoder receives information from each instruction source" does not provide any further limitations to the claimed invention since the predecoder certainly needs to receive information from each instruction source in order to predecode each instruction as claimed in claim 14. It is suggested to define the "instruction source" more specifically.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-22 are rejected under 35 U.S.C. 102(a) as being anticipated by Tran (USP 5,987,235) (Hereafter designated as Tran'235).

Referring to claim 1, Tran'235 discloses, as claimed, a method of handling a plurality of instructions within a processor (microprocessor 200, See Fig. 2) comprising: loading the plurality of instructions into a register (instruction

storage 302, see Fig. 3, note the instruction storage 302 is best reasonably and broadly interpreted as a register since it is a fast storage device inside the instruction cache 204 saving the instructions); determining the number and size of the plurality of instructions (see Col. 10, lines 30-32, regarding predecoder unit 203 decodes the instruction bytes to determine the number of instructions and length of each instruction); and decoding (by decode units 208 comprising 208A-208C, see Fig. 2, see also Col. 4, lines 34-35) the plurality of instructions.

Referring to claim 9, Tran'235 discloses, as claimed, a method of decoding a plurality of instructions within a processor (microprocessor 200, See Fig. 2) comprising: determining the size of the plurality of instructions (see Col. 10, lines 30-32, regarding predecoder unit 203 decodes the instruction bytes to determine the number of instructions and length of each instruction); presenting the plurality of instructions from an instruction register (instruction storage 302, see Fig. 3, note the instruction storage 302 is best reasonably and broadly interpreted as a register since it is a fast storage device inside the instruction cache 204 saving the instructions) to a decoder (decode units 208 comprising 208A-208C, see Fig. 2); and decoding each of the plurality of instructions within a single clock cycle (see Fig. 4D, for

example, in the single clock cycle 0, instructions 10, 11, and 12 are decoded by the decode units 208).

Referring to claim 14, Tran'235 discloses, as claimed, a processor (microprocessor 200, See Fig. 2) comprising: an instruction register (instruction storage 302, see Fig. 3, note the instruction storage 302 is best reasonably and broadly interpreted as a register since it is a fast storage device inside the instruction cache 204 saving the instructions) capable of holding a plurality of instructions; a pre-decoder (predecoder unit 203, see Fig. 2) which determines the size and number of the plurality of instructions (see Col. 10, lines 30-32, regarding predecoder unit 203 decodes the instruction bytes to determine the number of instructions and length of each instruction); and a decoder (decode units 208 comprising 208A-208C, see Fig. 2) which substantially simultaneously receives the plurality of instructions from the instruction register (see Fig. 4D, for example, in the single clock cycle 0, instructions 10, 11, and 12 are received by the decode units 208), wherein the decoder decodes each of the plurality of instructions within a single clock cycle (see Fig. 4D, for example, in the single clock cycle 0, instructions 10, 11, and 12 are decoded by the decode units 208).

Referring to claim 19, Tran'235 discloses, as claimed, an apparatus (microprocessor 200, See Fig. 2), including instructions residing on a machine-readable storage medium (main memory, see Fig. 2, and Col. 4 lines 66-67), for use in a machine system to handle a plurality of instructions, the instructions causing the machine to: determine the size of the plurality of instructions (see Col. 10, lines 30-32, regarding predecoder unit 203 decodes the instruction bytes to determine the number of instructions and length of each instruction); present the plurality of instructions from an instruction register (instruction storage 302, see Fig. 3, note the instruction storage 302 is best reasonably and broadly interpreted as a register since it is a fast storage device inside the instruction cache 204 saving the instructions) into a decoder (decode units 208 comprising 208A-208C, see Fig. 2); and decode each of the plurality of instructions within a single clock cycle (see Fig. 4D, for example, in the single clock cycle 0, instructions 10, 11, and 12 are decoded by the decode units 208).

As to claim 2, Tran'235 also discloses: decoding the plurality of instructions within a single clock cycle (see Fig. 4D, for example, in the single clock cycle 0, instructions 10, 11, and 12 are decoded by the decode units 208).

As to claim 3, Tran'235 also discloses: decoding the plurality of instructions substantially simultaneously (see Fig. 4D, for example, instructions 10, 11, and 12 are decoded by the decode units 208 in the single clock cycle 0 substantially simultaneously).

As to claim 4, Tran'235 also discloses: decoding width bits to determine the size of the instructions (see Fig. 4D, for example, instruction 10 has 3 instruction bytes and a size of 24 bits).

As to claim 5, Tran'235 also discloses: communicating the number and size of the plurality of instructions to the decoder (see Col. 10, lines 30-32, regarding predecoder unit 203 decodes the instruction bytes to determine the number of instructions and length of each instruction).

As to claim 6, Tran'235 also discloses: loading a first of the plurality of instructions having a first size (see Fig. 4B, instructions 10 and 12 each has a first size of 4 bytes (32 bits)) and a second of the plurality of instructions having a second size (see Fig. 4B, instructions 14 and 15 each has a second size of 2 bytes (16 bits)).

As to claim 7, Tran'235 also discloses: loading a first of the plurality of instructions having a first size (see Fig. 4B, instructions 10 and 12 each has a first size of 4 bytes (32

bits)), and loading a second and a third of the plurality of instructions having a second size (see Fig. 4B, instructions 14 and 15 each has a second size of 2 bytes (16 bits)), wherein the first size is 32-bits and the second size is 16-bits.

As to claims 8, 13, 18, and 22, Tran'235 also discloses: handling the plurality of instructions within a digital signal processor (microprocessor 200, See Fig. 2).

As to claims 10 and 20, Tran'235 also discloses: simultaneously presenting each of the plurality of instructions to the decoder (see Fig. 4D, for example, in the single clock cycle 0, instructions 10, 11, and 12 are received by the decode units 208; and see also Fig. 2, each of decode units 208A-208C of the decode units 208 has an individual bus connected with instruction alignment unit 206 for simultaneously presenting each of the plurality of instructions).

As to claims 11, 15, and 21, Tran'235 also discloses: decoding the plurality of instructions to determine the width of the plurality of instructions (see Col. 10, lines 30-32, regarding predecoder unit 203 decodes the instruction bytes to determine the number of instructions and length of each instruction).

As to claim 12, Tran'235 also discloses: a next plurality of instructions (such as instruction line 1, see Fig. 4A) into

the single instruction register (instruction storage 302, see Fig. 3).

As to claim 16, Tran'235 also discloses: the predecoder (predecoder unit 203, see Fig. 2) receives information from each instruction source (see Col. 10, lines 30-32, regarding predecoder unit 203 decodes the instruction bytes to determine the number of instructions and length of each instruction).

As to claim 17, Tran'235 also discloses: the predecoder (predecoder unit 203, see Fig. 2) communicates the number and size of the plurality of instructions to the decoder (decode units 208 comprising 208A-208C, see Fig. 2). See also Col. 10, lines 30-32, regarding predecoder unit 203 decodes the instruction bytes to determine the number of instructions and length of each instruction.

Conclusion

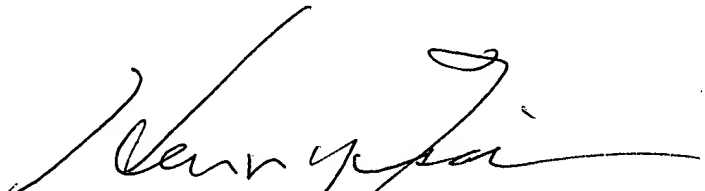
5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, such as Witt'6493; Favor'642; and Tran et al.'869 also disclosing the similar limitations as claimed.

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

7. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:** 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.



HENRY W. H. TSAI
PRIMARY EXAMINER
December 29, 2003